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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**APPLICANT(S):** SHAHAR, Arie et al.    **EXAMINER:** Not yet known  
**SERIAL NO.:** 10/813,108    **GROUP ART UNIT:** 2874  
**FILED:** March 31, 2004    **ATTORNEY DOCKET No.:** P-5864-US  
**FOR:** ALL OPTICAL LOGIC GATES

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

**REQUEST FOR CORRECTED FILING RECEIPT**

Sir:

Attached is a copy of the official filing receipt received from the U.S. Patent and Trademark Office in connection with the above-identified Application for which issuance of a corrected filing receipt is respectfully requested.

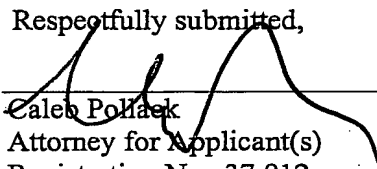
Also, attached is a copy of the Cross-Reference to Related Applications appearing in the specification of the application as filed.

There is an error in that the following data was omitted from the filing receipt:  
In addition to the data shown, this application is also a CIP of 10/404,140 filed on 04/02/2003

The correction or the error is not due to an error by Applicant(s) and no fee is due.

If any additional fee is required, the undersigned attorney hereby authorizes the Patent Office to charge such additional fee to Deposit Account 05-0649.

Respectfully submitted,

  
Caleb Pollack  
Attorney for Applicant(s)  
Registration No. 37,912

Dated: July 30, 2004

Eitan, Pearl, Latzer & Cohen Zedek, LLP.  
10 Rockefeller Plaza, Suite 1001  
New York, New York 10020  
Tel: (212) 632-3480  
Fax: (212) 632-3490



## UNITED STATES PATENT AND TRADEMARK OFFICE

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/813,108	03/31/2004	2874	550	P-5864-US	20	24	6

27130  
EITAN, PEARL, LATZER & COHEN ZEDEK LLP  
10 ROCKEFELLER PLAZA, SUITE 1001  
NEW YORK, NY 10020

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15 JUN 2004

CONFIRMATION NO. 5539

## FILING RECEIPT



\*0000000012933992\*

Date Mailed: 06/14/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Arie Shahar, Rye Brook, NY;  
Eldan Halberthal, Rye Brook, NY;

## Domestic Priority data as claimed by applicant

This appln claims benefit of 60/461,796 04/11/2003  
and is a CIP of 10/404,077 04/02/2003 *AMD is a CIP of 10/404,146 04/02/2003*  
which claims benefit of 60/405,697 08/22/2002

## Foreign Applications

If Required, Foreign Filing License Granted: 06/12/2004

Projected Publication Date: 09/23/2004

Non-Publication Request: No

Early Publication Request: No

\*\* SMALL ENTITY \*\*

## Title

All optical logic gates

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

**GRANTED**

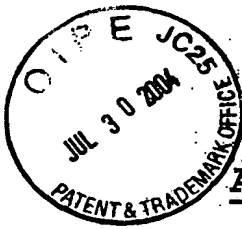
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## ALL OPTICAL LOGIC GATES

### **Cross-Reference To Related Applications**

This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/461,796, filed April 11, 2003, entitled "All Optical Logic Gates", and is a continuation in part of US Patent Applications Serial Numbers 10/404,077 and 10/404,140 filed April 2, 2003 entitled "Optical Threshold Devices and Methods". The latter application claims the benefit of US Provisional Patent Application Serial No. 60/405,697, filed August 22, 2002, entitled "Streaming signal control system for digital communications" now filed as four regular US Patent Applications Serial Numbers 10/640,035; 10/640,035; 10/640,017 and 10/640,040 filed August 14, 2003, entitled "All Optical Decoding Systems For Decoding Optical Encoded Data Symbols Across Multiple Decoding Layers", "All Optical Decoding Systems For Optical Encoded Data Symbols", "All Optical Cross Routing Using Decoding Systems For Optical Encoded Data Symbols" and "Compact Optical Delay Lines", respectively.

### **Field of Invention**

The invention relates to optical logic gates, optical communication devices and systems, optical computing devices and systems and in particular to optical AND gates, NAND gates and their combinations used to perform optical logic functions and gates.

### **Background of the Invention**

In the field of optical communication and optical computing there is a strong demand for optical gates capable of performing very fast execution of logic functions,